Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device, comprising:

a mounting substrate having a first main surface and a second main surface opposite the first main surface, wherein the mounting substrate is a single layer of resin material;

a step portion in the mounting substrate, at a periphery of the first main surface, wherein the step portion extends to about the middle of the mounting substrate in a thickness direction;

a first conductive pattern on the first main surface of the mounting substrate located inside the step portion;

a second conductive pattern on the second main surface of the mounting substrate;

a semiconductor element fixed to the first main surface of the mounting substrate and electrically connected to the first conductive pattern,

wherein the first conductive pattern extends under the semiconductor element and to the edge of the step portion; and

sealing resin covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element,

wherein a side surface of the sealing resin and a side surface of the mounting substrate are located on a same plane.

2. (Previously Presented) The semiconductor device according to claim 1, wherein the first conductive pattern comprises a bonding pad electrically connected to the semiconductor element through a fine metallic wire and a plating line extending from the bonding pad to the step portion.

3. (Original) The semiconductor device according to claim 2, wherein a plurality of the bonding pads are arranged so as to surround the semiconductor element, further comprising a wiring portion extending from each of the plurality of bonding pads under the semiconductor element.

4. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

forming first conductive patterns which constitute units and common plating lines on a front surface of a substrate, each of the units comprising bonding pads and plating lines extending from the respective bonding pads to a periphery, the common plating lines electrically connecting the plating lines of the units;

forming second conductive patterns on a back surface of the substrate, the second conductive patterns being electrically connected to the respective first conductive patterns;

forming a plated film to a surface of the first conductive patterns by electroplating using the common plating lines;

forming grooves on the front surface of the substrate by dicing the front surface of the substrate including the common plating lines to electrically separate the conductive patterns;

placing semiconductor elements on the front surface of the substrate;

providing sealing resin which fills the grooves and seals the semiconductor elements; and

separating the semiconductor elements by dicing the substrate and the sealing resin at borders of the units.

5. (Withdrawn) The method of manufacturing a semiconductor device according to claim 4, wherein the units are arranged in a matrix, and the common plating lines extend along the borders of the units into a grid.

6. (Previously Presented) The semiconductor device according to claim 1, wherein the mounting substrate comprises a resin.

7. (Previously Presented) The semiconductor device according to claim 1, wherein the second conductive pattern comprises electrodes arranged in a matrix.

8. (Currently Amended) A semiconductor device, comprising:

a mounting substrate having a first main surface and a second main surface opposite the first main surface, wherein the mounting substrate is a single layer of resin material;

a step portion in a periphery of the first main surface of the mounting substrate, wherein the step portion extends to about the middle of the mounting substrate in a thickness direction;

a first conductive pattern on the first main surface of the mounting substrate located inside the step portion,

wherein the first conductive pattern extends under the semiconductor element and to the edge of the step portion;

a second conductive pattern on the second main surface of the mounting substrate;

a semiconductor element fixed to the first main surface of the mounting substrate and electrically connected to the first conductive pattern; and

sealing resin covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element,

wherein an external side surface of the sealing resin and a side surface of the mounting substrate are located on a substantially same plane.

9. (Previously Presented) The semiconductor device according to claim 8, wherein the first conductive pattern comprises a bonding pad electrically connected to the semiconductor element through a fine metallic wire and a plating line extending from the bonding pad to the step portion.

10. (Previously Presented) The semiconductor device according to claim 9, wherein a plurality of the bonding pads are arranged so as to surround the semiconductor element, further

comprising a wiring portion extending from each of the plurality of bonding pads under the semiconductor element.

11. (Previously Presented) The semiconductor device according to claim 8, wherein the mounting substrate comprises a resin.

12. (Previously Presented) The semiconductor device according to claim 8, wherein the second conductive pattern comprises electrodes arranged in a matrix.

13. (Currently Amended) The semiconductor device according to claim 1, wherein the first conductive pattern extends laterally to the edge of the ~~of the~~ first main surface.

14. (Currently Amended) The semiconductor device according to claim 8, wherein the first conductive pattern extends laterally to the edge of the ~~of the~~ first main surface.

15. (New) The semiconductor device according to claim 1 wherein the semiconductor element is on the first conductive pattern and in direct in contact with a surface of the first conductive pattern.

16. (New) The semiconductor device according to claim 8 wherein the semiconductor element is on the first conductive pattern and in direct in contact with a surface of the first conductive pattern.